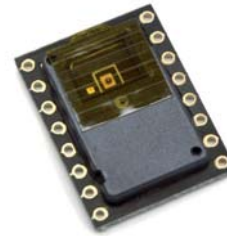


# ADNS-3530

## Low Power LED Integrated Slim Mouse Sensor



### Data Sheet



#### Description

The ADNS-3530 LED optical mouse sensor is a small form factor (SFF) LED illuminated navigation system.

The ADNS-3530 is a low-power optical navigation sensor. It has a new, low-power architecture and automatic power management modes, making it ideal for battery- and power-sensitive applications such as cordless input devices.

The ADNS-3530 is capable of high-speed motion detection — up to 20ips and 8g. In addition, it has an on-chip oscillator and integrated LED to minimize external components.

The ADNS-3530, along with the ADNS-3150-001 lens, forms a complete and compact mouse tracking system. There are no moving parts which means high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through a four-wire serial port. It is packaged in a 16 I/O surface mountable package.

#### Theory of Operation

The ADNS-3530 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADNS-3530 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the  $\Delta x$  and  $\Delta y$  relative displacement values.

An external microcontroller reads the  $\Delta x$  and  $\Delta y$  information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

#### Features

- Low power architecture
- Small form factor
- Surface mount technology (SMT) device
- Self-adjusting power-saving modes for longest battery life
- High speed motion detection up to 20 ips and 8g
- Self-adjusting frame rate for optimum performance
- Motion detect pin output
- Internal oscillator – no clock input needed
- Selectable 500 and 1000 cpi resolution
- Wide operating voltage: 2.7V - 3.6V nominal
- Four wire serial port
- Minimal number of passive components
- Integrated chip-on-board LED

#### Applications

- Optical mice
- Optical trackballs
- Integrated input devices
- Battery-powered input device

## Pinout of ADNS-3530 Optical Mouse Sensor

| Pin | Name    | Description                              |
|-----|---------|--|
| 1   | MISO    | Serial Data Output (Master In/Slave Out) |
| 2   | SCLK    | Serial Clock Input                       |
| 3   | MOSI    | Serial Data Input (Master Out/Slave In)  |
| 4   | MOTION  | Motion Detect (Active Low Output)        |
| 5   | XY_LED  | LED Control                              |
| 6   | LED_GND | Ground for LED Current                   |
| 7   | SHTDWN  | Shutdown (Active High Input)             |
| 8   | LED (+) | LED Positive Terminal                    |
| 9   | LED (-) | LED Negative Terminal                    |
| 10  | AVDD    | Analog Supply Voltage                    |
| 11  | GND     | Ground                                   |
| 12  | GND     | Ground                                   |
| 13  | AGND    | Analog Ground                            |
| 14  | VDD     | Supply Voltage                           |
| 15  | GND     | Ground                                   |
| 16  | NCS     | Chip Select (Active Low Input)           |

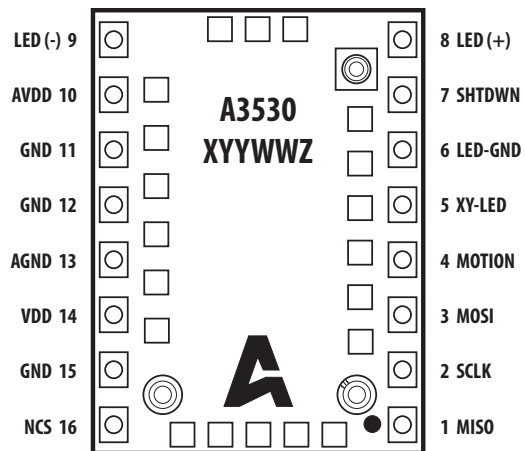
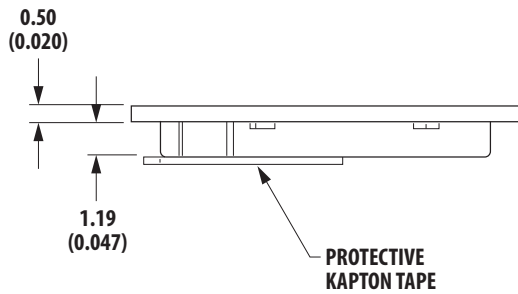
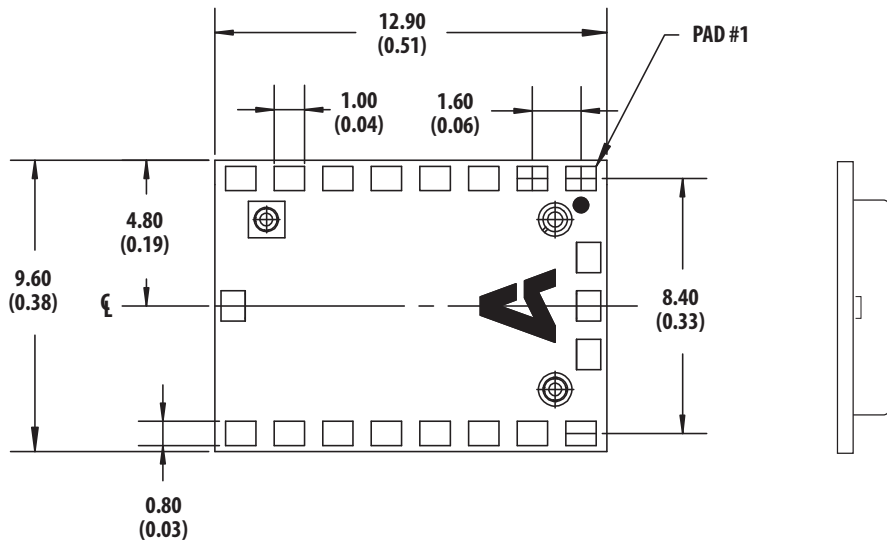


Figure 1. Package outline drawing (top view)



- NOTES:**
1. DIMENSIONS IN MILLIMETERS (INCHES).
  2. COPLANARITY OF PADS:  $\pm 0.1$  mm
  3. CUMULATIVE PITCH TOLERANCE:  $\pm 0.15$  mm
  4. PAD PITCH TOLERANCE:  $\pm 0.1$  mm
  5. MAXIMUM FLASH: + 0.2 mm
  6. DIMENSIONAL TOLERANCE (UNLESS OTHERWISE STATED):  $\pm 0.15$  mm

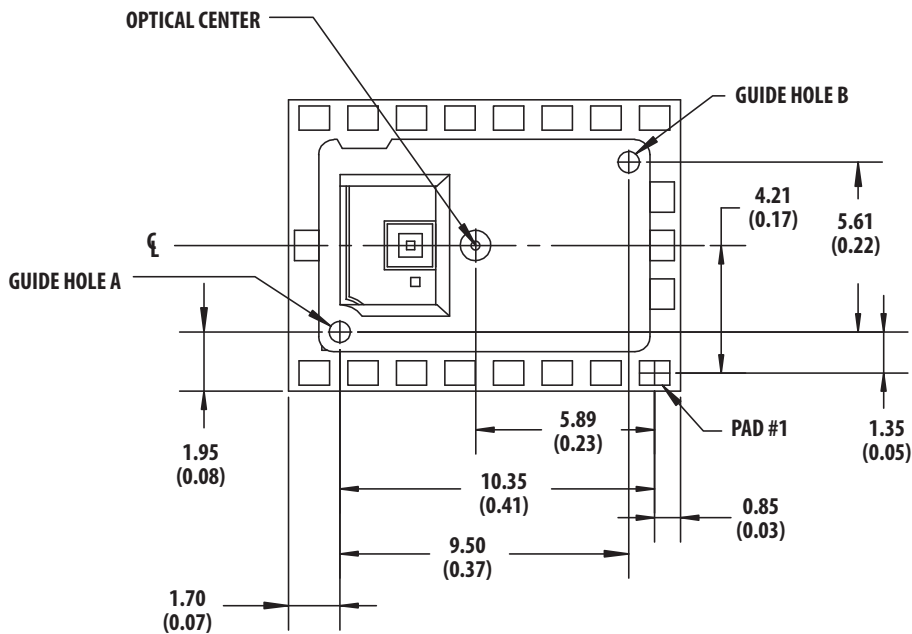


Figure 2. Package outline drawing

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

The components interlock as they are mounted onto defined features on the base plate.

The ADNS-3530 sensor is designed for surface mounting on a PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The ADNS-3150-001 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor and base plate.

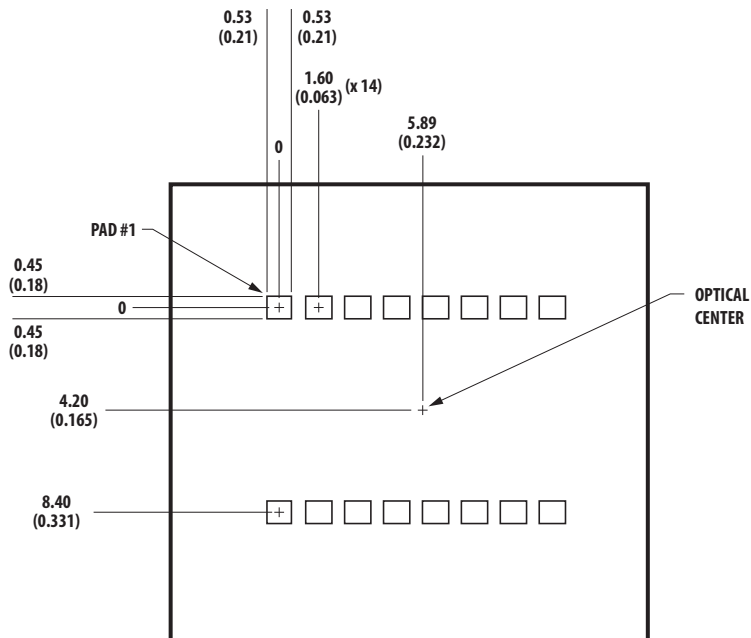


Figure 3. Recommended customer's PCB PADOUT and spacing

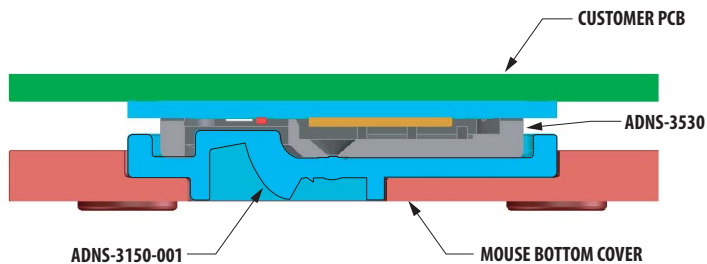


Figure 4. 2D assembly drawing of ADNS-3530

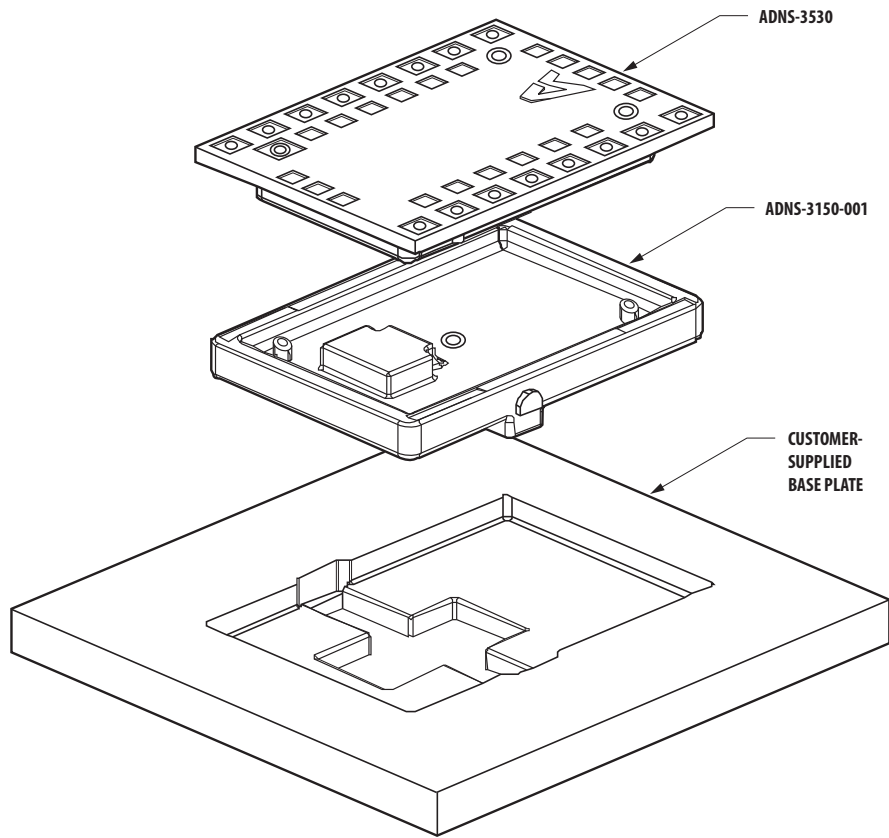


Figure 5a. Exploded top view

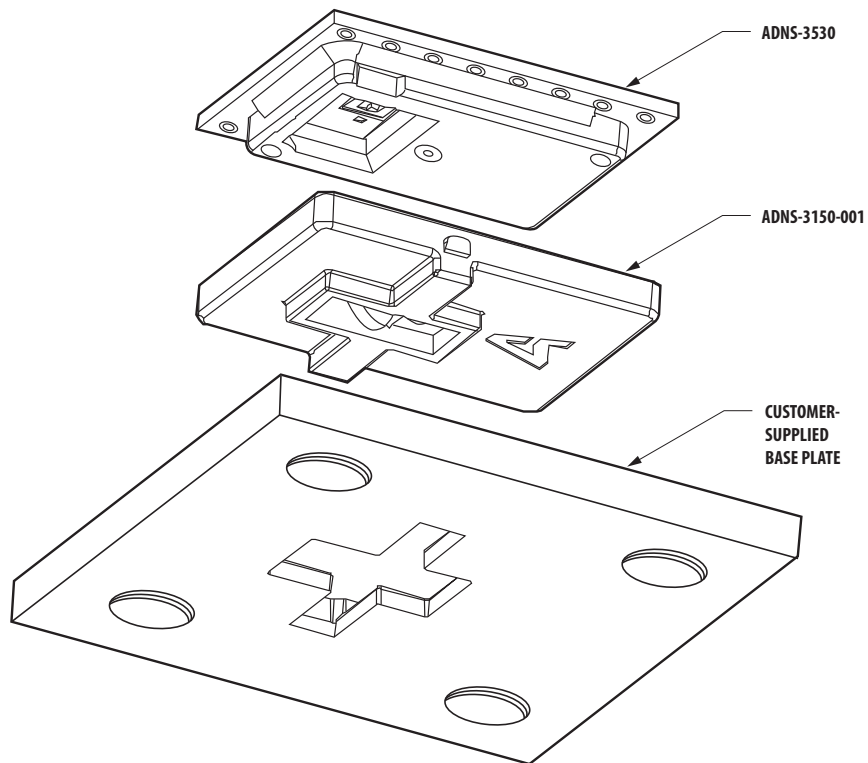


Figure 5b. Exploded bottom view

## PCB Assembly Considerations

1. Surface mount the sensor and all other electrical components into PCB.
2. Reflow the entire assembly in a no-wash solder process.
3. Place the lens onto the base plate. Care must be taken to avoid contaminating or staining the lens.
4. Remove the protective kapton tape from optical aperture of the sensor and LED. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
5. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The lens piece has alignment posts which will mate with the alignment holes on the sensor aperture.
6. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.

7. Install mouse top case. There MUST be a feature in the top case to press down onto the sensor to ensure the sensor and lens components are interlocked to the correct vertical height.

## Design Considerations for Improved ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago Technologies supplied IGES file and ADNS-3150-001 lens.

| Typical Distance | Millimeters |
|------------------|-------------|
| Creepage         | 0.6         |
| Clearance        | 2.76        |

Note that the lens material is polycarbonate and therefore, cyanoacrylate-based adhesives or other adhesives that may damage the lens should NOT be used.

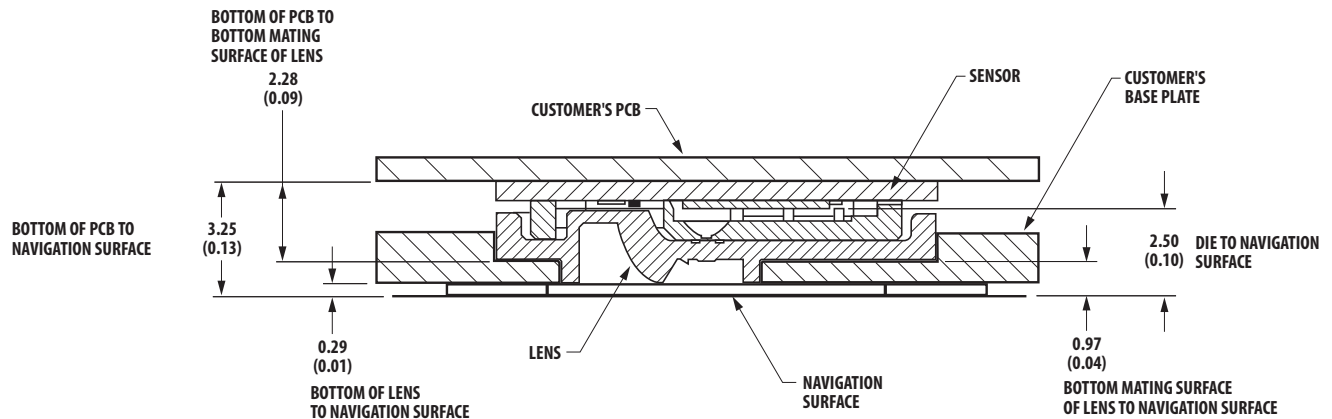


Figure 6a. Sectional view of PCB assembly

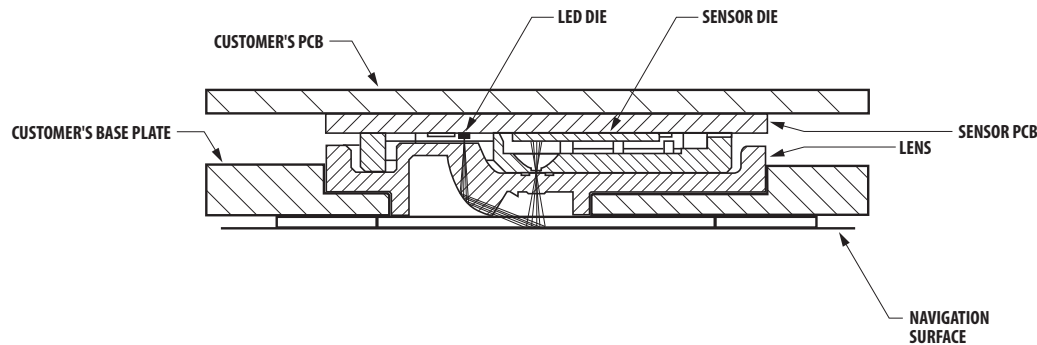


Figure 6b. Sectional view of PCB assembly highlighting optical mouse components

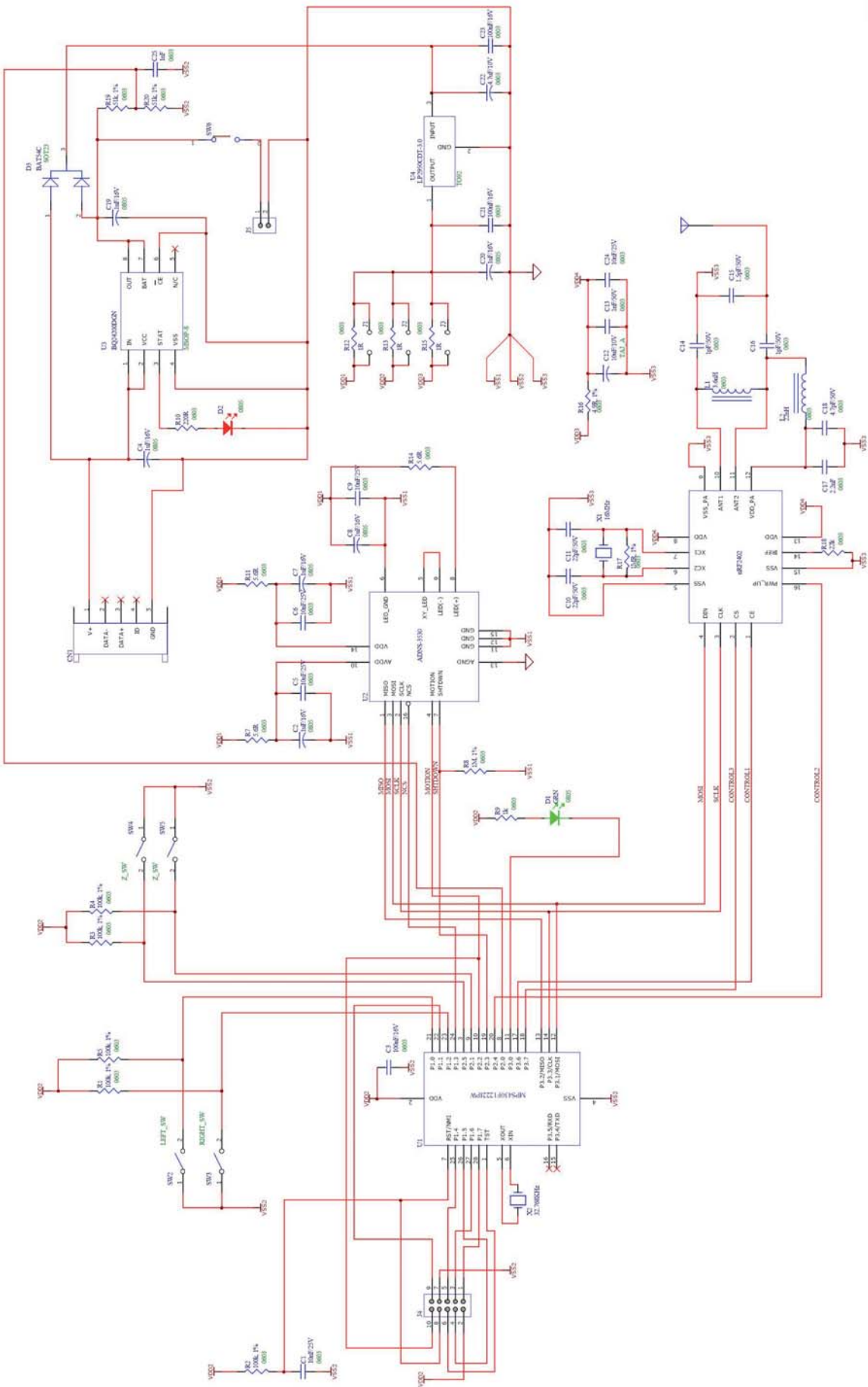


Figure 7. Schematic diagram for interface between ADNS-3530 and microcontroller

Note: The supply and ground paths should be laid out using a star topology.

## Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.

## Absolute Maximum Ratings

| Parameter               | Symbol           | Minimum | Maximum               | Units | Notes  |
|-------------------------|------------------|---------|-----------------------|-------|--|
| Storage Temperature     | T <sub>S</sub>   | -40     | 85                    | °C    |  |
| Lead Solder Temperature |                  |         | 260                   | °C    | For 10 seconds, 1.6 mm below seating plane     |
| Supply Voltage          | V <sub>DD</sub>  | -0.5    | 3.7                   | V     |  |
| ESD (Sensor Only)       |                  |         | 2                     | kV    | All pins, human body model MIL 883 Method 3015 |
| Input Voltage           | V <sub>IN</sub>  | -0.5    | V <sub>DD</sub> + 0.5 | V     | All pins                                       |
| Latchup Current         | I <sub>out</sub> |         | 20                    | mA    | All pins                                       |

## Recommended Operating Conditions

| Parameter                                     | Symbol            | Minimum | Typical | Maximum | Units  | Notes                        |
|---|-------------------|---------|---------|---------|--------|------------------------------|
| Operating Temperature                         | T <sub>A</sub>    | 0       |         | 40      | °C     |                              |
| Power Supply Voltage                          | V <sub>DD</sub>   | 2.7     |         | 3.6     | volts  | Including noise              |
| Power Supply Rise Time                        | V <sub>RT</sub>   | 0.001   |         | 100     | ms     | 0 to 2.8 V                   |
| Supply Noise (Sinusoidal)                     | V <sub>NA</sub>   |         |         | 100     | mVp-p  | 10 kHz - 50 MHz              |
| Serial Port Clock Frequency                   | f <sub>SCLK</sub> |         |         | 1       | MHz    | Active drive, 50% duty cycle |
| Distance from Lens Reference Plane to Surface | Z                 | -0.1    | 0.97    | +0.1    | mm     | Result in 0.1 mm DOF         |
| Speed   | S                 |         |         | 20      | in/sec |                              |
| Acceleration                                  | A                 |         |         | 8       | g      |                              |

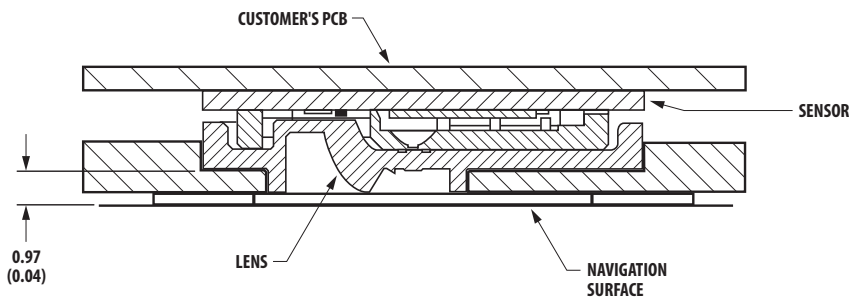


Figure 8. Distance from lens reference plane to surface



## AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V<sub>DD3</sub> = 2.85V.

| Parameter                                     | Symbol                               | Min. | Typical | Max.                | Units | Notes  |
|---|--------------------------------------|------|---------|---------------------|-------|--|
| Motion Delay After Reset                      | t <sub>MOT-RST</sub>                 |      |         | 23                  | ms    | From POWER_UP_RESET register write to valid motion, assuming motion is present   |
| Shutdown                                      | t <sub>SHTDWN</sub>                  |      |         | 50                  | ms    | From SHTDWN pin active to low current  |
| Wake from Shutdown                            | t <sub>WAKEUP</sub>                  | 1    |         |                     | s     | From SHTDWN pin inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown and Forced Rest," also note t <sub>MOT-RST</sub> |
| Forced Rest Enable                            | t <sub>REST-EN</sub>                 |      |         | 1                   | s     | From RESTEN bits set to low current  |
| Wake from Forced Rest                         | t <sub>REST-DIS</sub>                |      |         | 1                   | s     | From RESTEN bits cleared to valid motion   |
| MISO Rise Time                                | t <sub>r-MISO</sub>                  |      | 150     | 300                 | ns    | C <sub>L</sub> = 100 pF  |
| MISO Fall Time                                | t <sub>f-MISO</sub>                  |      | 150     | 300                 | ns    | C <sub>L</sub> = 100 pF  |
| MISO Delay After SCLK                         | t <sub>DLY-MISO</sub>                |      |         | 120                 | ns    | From SCLK falling edge to MISO data valid, no load conditions  |
| MISO Hold Time                                | t <sub>hold-MISO</sub>               | 0.5  |         | 1/f <sub>SCLK</sub> | μs    | Data held until next falling SCLK edge   |
| MOSI Hold Time                                | t <sub>hold-MOSI</sub>               | 200  |         |                     | ns    | Amount of time data is valid after SCLK rising edge  |
| MOSI Setup Time                               | t <sub>setup-MOSI</sub>              | 120  |         |                     | ns    | From data valid to SCLK rising edge  |
| SPI Time Between Write Commands               | t <sub>SWW</sub>                     | 30   |         |                     | μs    | From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte  |
| SPI Time Between Write and Read Commands      | t <sub>SWR</sub>                     | 20   |         |                     | μs    | From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte   |
| SPI Time Between Read and Subsequent Commands | t <sub>SRW</sub><br>t <sub>SRR</sub> | 500  |         |                     | ns    | From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command  |
| SPI Read Address-Data Delay                   | t <sub>SRAD</sub>                    | 4    |         |                     | μs    | From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read  |
| NCS Inactive After Motion Burst               | t <sub>BEXIT</sub>                   | 500  |         |                     | ns    | Minimum NCS inactive time after motion burst before next SPI usage   |
| NCS to SCLK Active                            | t <sub>NCS-SCLK</sub>                | 120  |         |                     | ns    | From NCS falling edge to first SCLK rising edge  |
| SCLK to NCS Inactive (for Read Operation)     | t <sub>SCLK-NCS</sub>                | 120  |         |                     | ns    | From last SCLK rising edge to NCS rising edge, for valid MISO data transfer  |
| SCLK to NCS Inactive (for Write Operation)    | t <sub>SCLK-NCS</sub>                | 20   |         |                     | us    | From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer  |
| NCS to MISO High-Z                            | t <sub>NCS-MISO</sub>                |      |         | 500                 | ns    | From NCS rising edge to MISO high-Z state  |
| MOTION Rise Time                              | t <sub>r-MOTION</sub>                |      | 150     | 300                 | ns    | C <sub>L</sub> = 100 pF  |
| MOTION Fall Time                              | t <sub>f-MOTION</sub>                |      | 150     | 300                 | ns    | C <sub>L</sub> = 100 pF  |
| SHTDWN Pulse Width                            | t <sub>p-SHTDWN</sub>                | 1    |         |                     | s     |  |
| Transient Supply Current                      | I <sub>DDT</sub>                     |      |         | 45                  | mA    | Max supply current during a V <sub>DD</sub> ramp from 0 to 2.8 V   |

## DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V<sub>DD</sub>=2.85 V.

| Parameter                          | Symbol                  | Min.                  | Typical | Max. | Units | Notes  |
|------------------------------------|-------------------------|-----------------------|---------|------|-------|--|
| DC Supply Current in Various Modes | I <sub>DD_RUN</sub>     |                       | 3.6     | 10   | mA    | Average current, including LED current.  |
|                                    | I <sub>DD_REST1</sub>   |                       | 0.6     | 1.8  |       | No load on MISO, MOTION.   |
|                                    | I <sub>DD_REST2</sub>   |                       | 0.15    | 0.40 |       |  |
|                                    | I <sub>DD_REST3</sub>   |                       | 0.04    | 0.15 |       |  |
| Peak Supply Current                |                         |                       |         | 40   | mA    | Peak current in 100 kHz bandwidth, including LED current.  |
| Shutdown Supply Current            | I <sub>DDSHUTDOWN</sub> |                       | 1       | 12   | µA    | SCLK, MOSI and NCS must be within 300 mV of GND or V <sub>DD</sub> . SHTDWN must be within 300 mV of V <sub>DD</sub> . |
| Input Low Voltage                  | V <sub>IL</sub>         |                       |         | 0.5  | V     | SCLK, MOSI, NCS, SHTDWN  |
| Input High Voltage                 | V <sub>IH</sub>         | V <sub>DD</sub> - 0.6 |         |      | V     | SCLK, MOSI, NCS, SHTDWN  |
| Input Hysteresis                   | V <sub>I_HYS</sub>      |                       | 100     |      | mV    | SCLK, MOSI, NCS, SHTDWN  |
| Input Leakage Current              | I <sub>leak</sub>       |                       | ±1      | ±10  | µA    | V <sub>in</sub> = V <sub>DD</sub> - 0.6V, SCLK, MOSI, NCS, SHTDWN  |
| Output Low Voltage                 | V <sub>OL</sub>         |                       |         | 0.7  | V     | I <sub>out</sub> = 1 mA, MISO, MOTION  |
| Output High Voltage                | V <sub>OH</sub>         | V <sub>DD</sub> - 0.7 |         |      | V     | I <sub>out</sub> = -1 mA, MISO, MOTION   |
| Input Capacitance                  | C <sub>in</sub>         |                       |         | 10   | pF    | MOSI, NCS, SCLK, SHTDWN  |

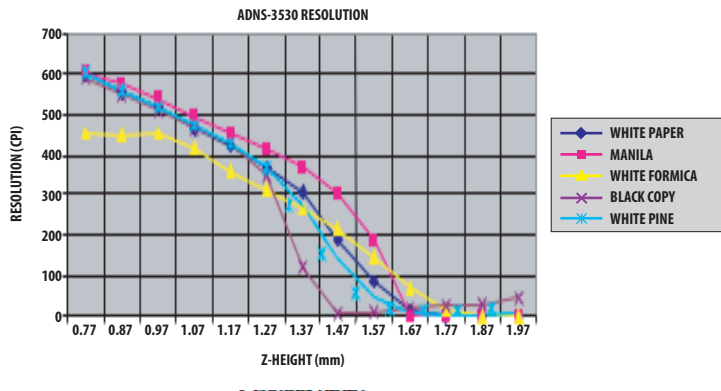


Figure 9. Mean resolution vs. Z

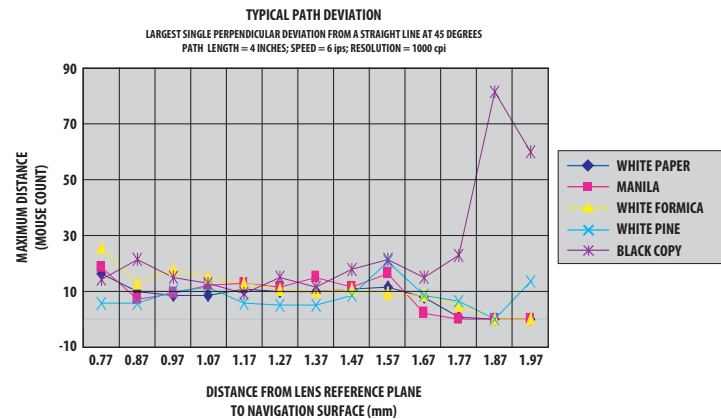


Figure 10. Typical path deviation vs. Z distance (mm)

Relationship of mouse count to distance =  $m$  (mouse count)/ $n$  (cpi). E.g.: Deviation of 7 mouse count =  $7/1000 = 0.007$  inch, where  $m = 7$ ,  $n = 1000$ .

## Power Management Modes

The ADNS-3530 has three power-saving modes. Each mode has a different motion detection period, affecting response time to mouse motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

| Mode   | Response Time (Nominal) | Downshift Time (Nominal) |
|--------|-------------------------|--------------------------|
| Rest 1 | 16.5 ms                 | 237 ms                   |
| Rest 2 | 82 ms                   | 8.4 s                    |
| Rest 3 | 410 ms                  | 504 s                    |

## Motion Pin Timing

The motion pin is a level-sensitive output that signals the microcontroller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta\_X or Delta\_Y registers. Clearing the motion bit (by reading Delta\_Y and Delta\_X, or writing to the Motion register) will put the motion pin high.

## LED Mode

For power savings, the LED will not be continuously on. ADNS-3530 will flash the LED only when needed.

## Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-3530, and to read out the motion information.

The port is a four wire serial port. The host microcontroller always initiates communication; the ADNS-3530 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a microcontroller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the microcontroller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

## Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

## Write Operation

Write operation, defined as data going from the microcontroller to the ADNS-3530, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-3530 reads MOSI on rising edges of SCLK.

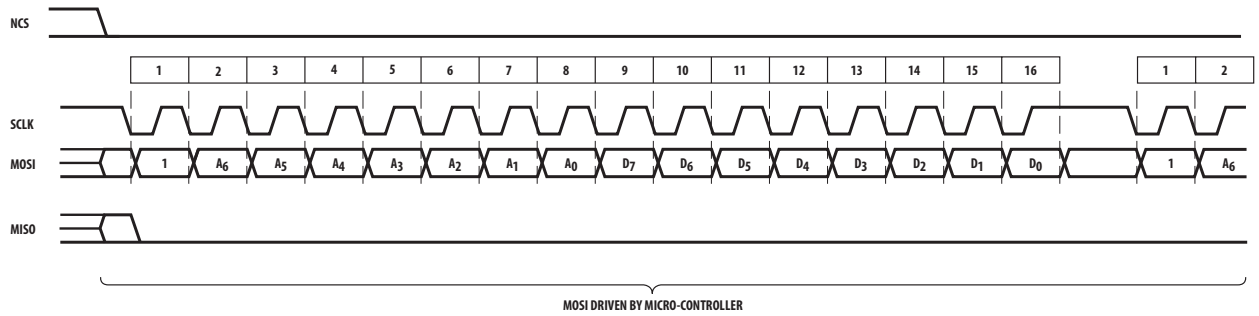


Figure 11. Write operation

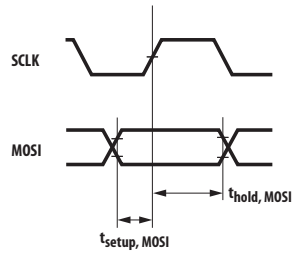


Figure 12. MOSI setup and hold time

### Read Operation

A read operation, defined as data going from the ADNS-3530 to the microcontroller, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address, is sent by the microcontroller over MOSI, and has a “0” as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-3530 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

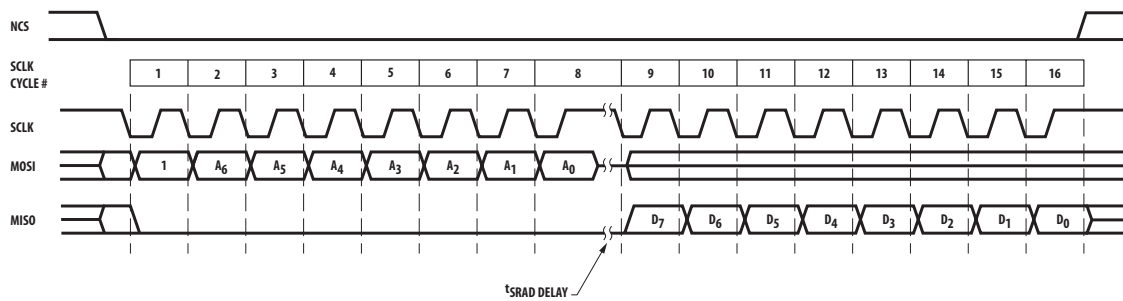


Figure 13. Read operation

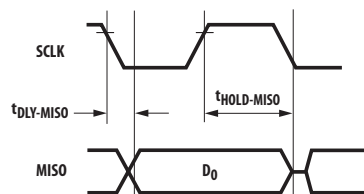
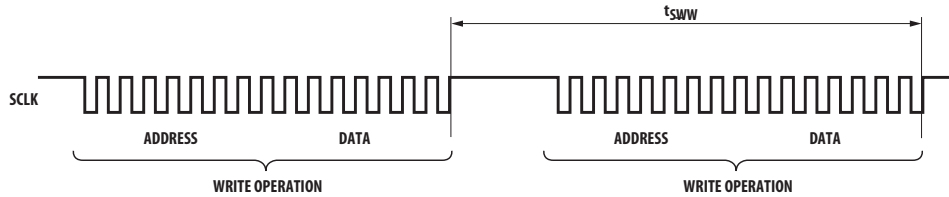


Figure 14. MISO delay and hold time

NOTE: The  $0.5/f_{SCLK}$  minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-3530. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-3530 will hold the state of data on MISO until the falling edge of SCLK.

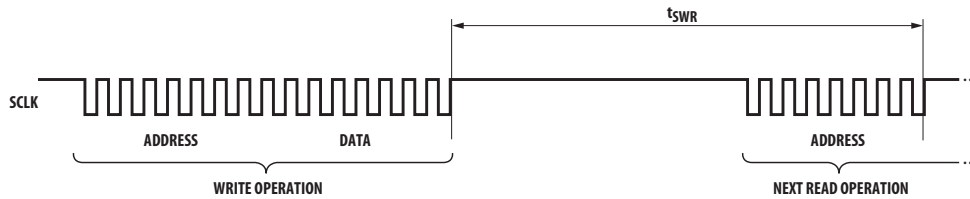
**Required Timing Between Read and Write Commands**

There are minimum timing requirements between read and write commands on the serial port.



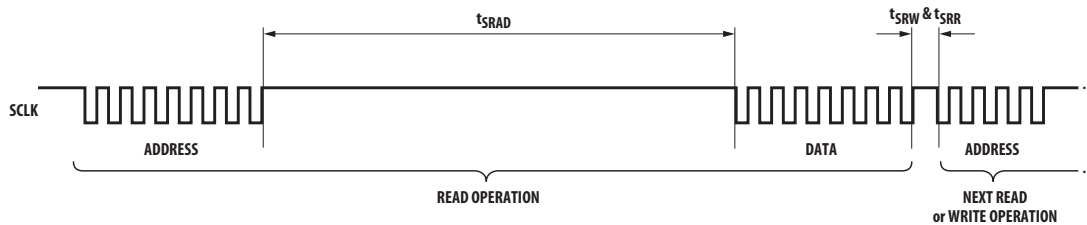
**Figure 15. Timing between two write commands**

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay ( $t_{SWW}$ ), then the first write command may not complete correctly.



**Figure 16. Timing between write and read commands**

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay ( $t_{SWR}$ ), the write command may not complete correctly.



**Figure 17. Timing between read and either write or subsequent read commands**

During a read operation SCLK should be delayed at least  $t_{SRAD}$  after the last address data bit to ensure that the ADNS-3530 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least  $t_{SRR}$  or  $t_{SRW}$  after the last SCLK rising edge of the last data bit of the previous read operation.

### Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion\_Burst register. The ADNS-3530 will respond with the contents of the Motion, Delta\_Y, Delta\_X, SQUAL, Shutter\_Upper, Shutter\_Lower and Maximum\_Pixel registers in that order. The burst transaction can be terminated after the first three bytes of the sequence are read by bringing the NCS pin high. After sending the register address, the microcontroller must wait  $t_{SRAD}$  and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the microcontroller must raise the NCS line for at least  $t_{BEXIT}$  to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

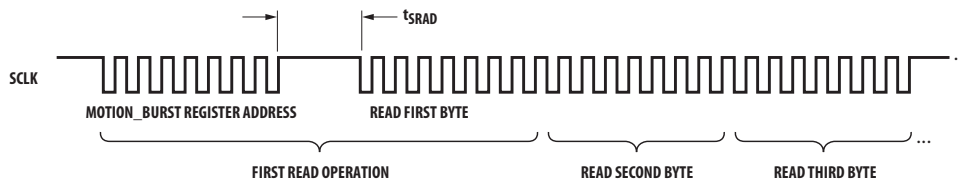


Figure 18. Motion burst timing

### Notes on Power-Up

The ADNS-3530 does not perform an internal power up self-reset; the POWER\_UP\_RESET register must be written every time power is applied. The appropriate sequence is as follows:

1. Apply power
2. Drive NCS high, then low to reset the SPI port
3. Write 0x5a to register 0x3a

4. Read from registers 0x02, 0x03 and 0x04 (or read these same three bytes from burst motion register 0x42) one time regardless the state of the motion pin.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

| State of Signal Pins After VDD is Valid |             |                       |                      |                |
|---|-------------|-----------------------|----------------------|----------------|
| Pin                                     | On Power-Up | NCS High Before Reset | NCS Low Before Reset | After Reset    |
| NCS                                     | Functional  | High                  | Low                  | Functional     |
| MISO                                    | Undefined   | Undefined             | Functional           | Depends on NCS |
| SCLK                                    | Ignored     | Ignored               | Functional           | Depends on NCS |
| MOSI                                    | Ignored     | Ignored               | Functional           | Depends on NCS |
| XY_LED                                  | Undefined   | Undefined             | Undefined            | Functional     |
| MOTION                                  | Undefined   | Undefined             | Undefined            | Functional     |
| SHTDWN                                  | Must Be Low | Must Be Low           | Must Be Low          | Functional     |

### Notes on Shutdown and Forced Rest

The ADNS-3530 can be set in Rest mode through the Configuration\_Bits register (0x11). This is to allow for further power savings in applications where the sensor does not need to operate all the time.

The ADNS-3530 can be set in Shutdown mode by asserting the SHTDWN pin. For proper operation, SHTDWN pulse width must be at least  $t_{SHTDWN}$ . Shorter pulse widths may cause the chip to enter an undefined state. In addition, the SPI port should not be accessed when SHTDWN is asserted. (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. After deasserting SHTDWN, a full reset must be initiated. Wait  $t_{WAKEUP}$  before accessing the SPI port, then write 0x5A to the POWER\_UP\_RESET register. Any register settings must then be reloaded.

| Pin    | SHTDWN active |
|--------|---------------|
| NCS    | Functional*   |
| MISO   | Undefined     |
| SCLK   | Undefined     |
| MOSI   | Undefined     |
| XY_LED | Low Current   |
| MOTION | Undefined     |

\*NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It can be in either state if the sensor is the only device in addition to the microcontroller.

**Note:** There are long wakeup times from shutdown and forced Rest. These features should not be used for power management during normal mouse motion.

## Registers

The ADNS-3530 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

| Address   | Register            | Read/Write | Default Value |
|-----------|---------------------|------------|---------------|
| 0x00      | Product_ID          | R          | 0x0D          |
| 0x01      | Revision_ID         | R          | 0x02          |
| 0x02      | Motion              | R/W        | 0x00          |
| 0x03      | Delta_Y             | R          | Any           |
| 0x04      | Delta_X             | R          | Any           |
| 0x05      | SQUAL               | R          | Any           |
| 0x06      | Shutter_Upper       | R          | Any           |
| 0x07      | Shutter_Lower       | R          | Any           |
| 0x08      | Maximum_Pixel       | R          | Any           |
| 0x09      | Pixel_Sum           | R          | Any           |
| 0x0a      | Minimum_Pixel       | R          | Any           |
| 0x0b      | Pixel_Grab          | R/W        | Any           |
| 0x0c      | CRC0                | R          | Any           |
| 0x0d      | CRC1                | R          | Any           |
| 0x0e      | CRC2                | R          | Any           |
| 0x0f      | CRC3                | R          | Any           |
| 0x10      | Self_Test           | W          |               |
| 0x11      | Configuration_Bits  | R/W        | 0x03          |
| 0x12-0x2d | Reserved            |            |               |
| 0x2e      | Observation         | R/W        | Any           |
| 0x2f-0x38 | Reserved            |            |               |
| 0x3a      | POWER_UP_RESET      | W          |               |
| 0x3b-0x3d | Reserved            |            |               |
| 0x3e      | Inverse_Revision_ID | R          | 0xFD          |
| 0x3f      | Inverse_Product_ID  | R          | 0xF2          |
| 0x42      | Motion_Burst        | R          | Any           |

**Product\_ID** Address: 0x00

Access: Read Reset Value: 0x0D

|       |                  |                  |                  |                  |                  |                  |                  |                  |
|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit   | 7                | 6                | 5                | 4                | 3                | 2                | 1                | 0                |
| Field | PID <sub>7</sub> | PID <sub>6</sub> | PID <sub>5</sub> | PID <sub>4</sub> | PID <sub>3</sub> | PID <sub>2</sub> | PID <sub>1</sub> | PID <sub>0</sub> |

Data Type: 8-bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-3530. The value in this register does not change; it can be used to verify that the serial communications link is functional.



**Revision\_ID** Address: 0x01  
 Access: Read Reset Value: 0x02

|       |                  |                  |                  |                  |                  |                  |                  |                  |
|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit   | 7                | 6                | 5                | 4                | 3                | 2                | 1                | 0                |
| Field | RID <sub>7</sub> | RID <sub>6</sub> | RID <sub>5</sub> | RID <sub>4</sub> | RID <sub>3</sub> | RID <sub>2</sub> | RID <sub>1</sub> | RID <sub>0</sub> |

Data Type: 8-bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

**Motion** Address: 0x02  
 Access: Read/Write Reset Value: 0x00

|       |     |        |          |     |          |          |          |          |
|-------|-----|--------|----------|-----|----------|----------|----------|----------|
| Bit   | 7   | 6      | 5        | 4   | 3        | 2        | 1        | 0        |
| Field | MOT | PIXRDY | PIXFIRST | OVF | Reserved | Reserved | Reserved | Reserved |

Data Type: bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta\_Y and Delta\_X registers.

Writing anything to this register clears the MOT and OVF bits, Delta\_Y and Delta\_X registers. The written data byte is not saved.

Internal buffers can accumulate more than eight bits of motion for X or Y. If either one of the internal buffers overflows, then absolute path data is lost and the OVF bit is set. This bit is cleared once some motion has been read from the Delta\_X and Delta\_Y registers, and if the buffers are not at full scale. Since more data is present in the buffers, the cycle of reading the Motion, Delta\_X and Delta\_Y registers should be repeated until the motion bit (MOT) is cleared. Until MOT is cleared, either the Delta\_X or Delta\_Y registers will read either positive or negative full scale. If the motion register has not been read for long time, at 500 cpi it may take up to 16 read cycles to clear the buffers, at 1000 cpi, up to 32 cycles. To clear an overflow, write anything to this register.

The PIXRDY bit will be set whenever a valid pixel data byte is available in the Pixel\_Dump register. Check that this bit is set before reading from Pixel\_Dump. To ensure that the Pixel\_Grab pointer has been reset to pixel 0,0 on the initial write to Pixel\_Grab, check to see if PIXFIRST is set to high.

| Field Name | Description  |
|------------|--|
| MOT        | Motion since last report<br><b>0 = No motion</b><br>1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers   |
| PIXRDY     | Pixel Dump data byte is available in Pixel_Dump register<br><b>0 = data not available</b><br>1 = data available  |
| PIXFIRST   | This bit is set when the Pixel_Grab register is written to or when the complete pixel array has been read, initiating an increment to pixel 0,0.<br><b>0 = Pixel_Grab data not from pixel 0,0</b><br>1 = Pixel_Grab data is from pixel 0,0 |
| OVF        | Motion overflow, _Y and/or _X buffer has overflowed since last report<br><b>0 = no overflow</b><br>1 = Overflow has occurred   |

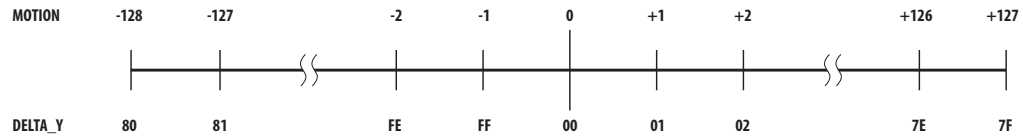
**Delta\_Y** Address: 0x03

Access: Read Reset Value: Undefined

|       |                |                |                |                |                |                |                |                |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit   | 7              | 6              | 5              | 4              | 3              | 2              | 1              | 0              |
| Field | X <sub>7</sub> | X <sub>6</sub> | X <sub>5</sub> | X <sub>4</sub> | X <sub>3</sub> | X <sub>2</sub> | X <sub>1</sub> | X <sub>0</sub> |

Data Type: Eight bit 2's complement number

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

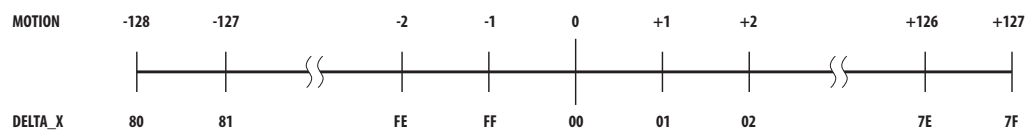
**Delta\_X** Address: 0x04

Access: Read Reset Value: Undefined

|       |                |                |                |                |                |                |                |                |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit   | 7              | 6              | 5              | 4              | 3              | 2              | 1              | 0              |
| Field | Y <sub>7</sub> | Y <sub>6</sub> | Y <sub>5</sub> | Y <sub>4</sub> | Y <sub>3</sub> | Y <sub>2</sub> | Y <sub>1</sub> | Y <sub>0</sub> |

Data Type: Eight bit 2's complement number

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

---

**SQUAL** Address: 0x05

Access: Read Reset Value: Undefined

|       |                 |                 |                 |                 |                 |                 |                 |                 |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit   | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Field | SQ <sub>7</sub> | SQ <sub>6</sub> | SQ <sub>5</sub> | SQ <sub>4</sub> | SQ <sub>3</sub> | SQ <sub>2</sub> | SQ <sub>1</sub> | SQ <sub>0</sub> |

Data Type: Upper 8 bits of a 9-bit unsigned integer

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame. The maximum SQUAL register value is 167. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected.

---

**Shutter\_Upper** Address: 0x06

Access: Read Reset Value: Undefined

|       |                 |                 |                 |                 |                 |                 |                |                |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| Bit   | 7               | 6               | 5               | 4               | 3               | 2               | 1              | 0              |
| Field | S <sub>15</sub> | S <sub>14</sub> | S <sub>13</sub> | S <sub>12</sub> | S <sub>11</sub> | S <sub>10</sub> | S <sub>9</sub> | S <sub>8</sub> |

**Shutter\_Lower** Address: 0x07

Access: Read Reset Value: Undefined

|       |                |                |                |                |                |                |                |                |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit   | 7              | 6              | 5              | 4              | 3              | 2              | 1              | 0              |
| Field | S <sub>7</sub> | S <sub>6</sub> | S <sub>5</sub> | S <sub>4</sub> | S <sub>3</sub> | S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> |

Data Type: Sixteen bit unsigned integer

USAGE: Units are clock cycles. Read Shutter\_Upper first, then Shutter\_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

---

**Maximum\_Pixel** Address: 0x08

Access: Read Reset Value: Undefined

|       |                 |                 |                 |                 |                 |                 |                 |                 |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit   | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Field | MP <sub>7</sub> | MP <sub>6</sub> | MP <sub>5</sub> | MP <sub>4</sub> | MP <sub>3</sub> | MP <sub>2</sub> | MP <sub>1</sub> | MP <sub>0</sub> |

Data Type: Eight-bit number

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

**Pixel\_Sum** Address: 0x09

Access: Read Reset Value: Undefined

|       |                 |                 |                 |                 |                 |                 |                 |                 |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit   | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Field | AP <sub>7</sub> | AP <sub>6</sub> | AP <sub>5</sub> | AP <sub>4</sub> | AP <sub>3</sub> | AP <sub>2</sub> | AP <sub>1</sub> | AP <sub>0</sub> |

Data Type: High 8 bits of an unsigned 17-bit integer

USAGE: This register is used to find the average pixel value. It reports the seven bits of a 16-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value, use the following formula:

$$\text{Average Pixel} = \text{Register Value} * 128/121 = \text{Register Value} * 1.06$$

The maximum register value is 240. The minimum is 0. The pixel sum value can change on every frame.

---

**Minimum\_Pixel** Address: 0x0a

Access: Read Reset Value: Undefined

|       |                 |                 |                 |                 |                 |                 |                 |                 |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit   | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Field | MP <sub>7</sub> | MP <sub>6</sub> | MP <sub>5</sub> | MP <sub>4</sub> | MP <sub>3</sub> | MP <sub>2</sub> | MP <sub>1</sub> | MP <sub>0</sub> |

Data Type: Eight-bit number

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value can vary with every frame.

---

**Pixel\_Grab** Address: 0x0b

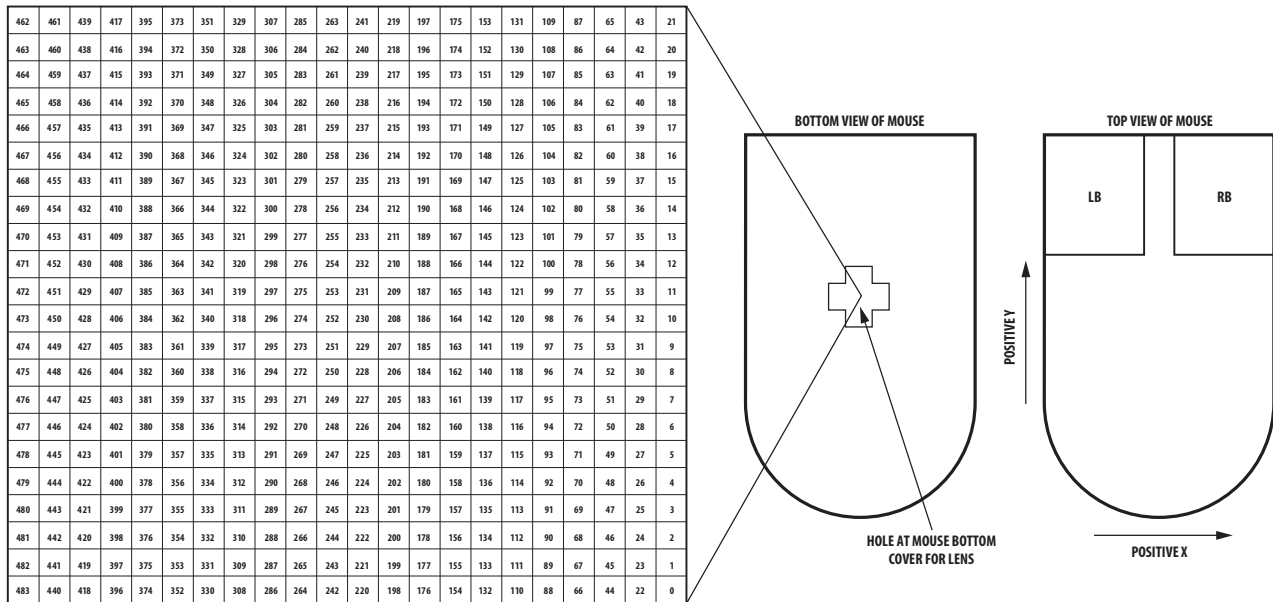
Access: Read/Write Reset Value: Undefined

|       |                 |                 |                 |                 |                 |                 |                 |                 |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit   | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Field | PD <sub>7</sub> | PD <sub>6</sub> | PD <sub>5</sub> | PD <sub>4</sub> | PD <sub>3</sub> | PD <sub>2</sub> | PD <sub>1</sub> | PD <sub>0</sub> |

Data Type: Eight-bit word

USAGE: For test purposes, the sensor will read out the contents of the pixel array, one pixel per frame. To start a pixel grab, write anything to this register to reset the pointer to pixel 0,0. Then read the PIXRDY bit in the Motion register. When the PIXRDY bit is set, there is valid data in this register to read out. After the data in this register is read, the pointer will automatically increment to the next pixel. Reading may continue indefinitely; once a complete frame's worth of pixels has been read, PIXFIRST will be set to high to indicate the start of the first pixel and the address pointer will start at the beginning location again.

**(Pixel Array Map Looking Through the ADNS-3150-001 Lens)**



**Figure 19. Surface image pixel address map**

**CRC0** Address: 0x0c

Access: Read Reset Value: Undefined

|       |                   |                   |                   |                   |                   |                   |                   |                   |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit   | 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| Field | CRC0 <sub>7</sub> | CRC0 <sub>6</sub> | CRC0 <sub>5</sub> | CRC0 <sub>4</sub> | CRC0 <sub>3</sub> | CRC0 <sub>2</sub> | CRC0 <sub>1</sub> | CRC0 <sub>0</sub> |

Data Type: Eight-bit number

USAGE: Register 0x0c reports the first byte of the system self test results. Value = 0xAF. See Self Test register 0x10.

**CRC1** Address: 0x0d

Access: Read Reset Value: Undefined

|       |                   |                   |                   |                   |                   |                   |                   |                   |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit   | 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| Field | CRC1 <sub>7</sub> | CRC1 <sub>6</sub> | CRC1 <sub>5</sub> | CRC1 <sub>4</sub> | CRC1 <sub>3</sub> | CRC1 <sub>2</sub> | CRC1 <sub>1</sub> | CRC1 <sub>0</sub> |

Data Type: Eight bit number

USAGE: Register 0x0c reports the second byte of the system self test results. Value = 0x4E. See Self Test register 0x10.

**CRC2** Address: 0x0e

Access: Read Reset Value: Undefined

|       |                   |                   |                   |                   |                   |                   |                   |                   |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit   | 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| Field | CRC2 <sub>7</sub> | CRC2 <sub>6</sub> | CRC2 <sub>5</sub> | CRC2 <sub>4</sub> | CRC2 <sub>3</sub> | CRC2 <sub>2</sub> | CRC2 <sub>1</sub> | CRC2 <sub>0</sub> |

Data Type: Eight-bit number

USAGE: Register 0x0e reports the third byte of the system self test results. Value = 0x31. See Self Test register 0x10.

**CRC3** Address: 0x0f

Access: Read Reset Value: Undefined

|       |                   |                   |                   |                   |                   |                   |                   |                   |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit   | 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| Field | CRC3 <sub>7</sub> | CRC3 <sub>6</sub> | CRC3 <sub>5</sub> | CRC3 <sub>4</sub> | CRC3 <sub>3</sub> | CRC3 <sub>2</sub> | CRC3 <sub>1</sub> | CRC3 <sub>0</sub> |

Data Type: Eight-bit number

USAGE: Register 0x0f reports the fourth byte of the system self test results. Value = 0x22. See Self Test register 0x10.

**Self\_Test** Address: 0x10

Access: Write Reset Value: NA

|       |          |          |          |          |          |          |          |        |
|-------|----------|----------|----------|----------|----------|----------|----------|--------|
| Bit   | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0      |
| Field | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | TESTEN |

Data Type: Bit field

USAGE: Set the TESTEN bit in register 0x10 to start the system self-test. The test takes 250 ms. During this time, do not write or read through the SPI port. Results are available in the CRC0-3 registers. After self-test, reset the chip to start normal operation.

| Field Name | Description  |
|------------|--|
| TESTEN     | Enable System Self Test<br><b>0 = Disabled</b><br>1 = Enable |

**Configuration\_bits** Address: 0x11

Access: Read/Write Reset Value: 0x03

|       |     |          |             |             |          |          |          |          |
|-------|-----|----------|-------------|-------------|----------|----------|----------|----------|
| Bit   | 7   | 6        | 5           | 4           | 3        | 2        | 1        | 0        |
| Field | RES | Reserved | RESTEN<br>1 | RESTEN<br>0 | Reserved | Reserved | Reserved | Reserved |

Data Type: Bit field

USAGE: Register 0x11 allows the user to change the configuration of the sensor. Setting the RESTEN bit forces the sensor into Rest mode, as described in the power modes section above. The RES bit allows selection between 500 and 1000 cpi resolution.

*Note: Forced Rest has a long wakeup time and should not be used for power management during normal mouse motion.*

| Field Name            | Description  |
|-----------------------|--|
| RESTEN <sub>1-0</sub> | Puts chip into Rest mode<br><b>00 = normal operation</b><br>01 = force Rest1<br>10 = force Rest2<br>11 = force Rest3 |
| RES                   | Sets resolution<br><b>0 = 500</b><br>1 = 1000  |

---

**Reserved** Address: 0x12-0x2d

**Observation** Address: 0x2e

Access: Read/Write Reset Value: Undefined

|       |                   |                   |          |          |                  |                  |                  |                  |
|-------|-------------------|-------------------|----------|----------|------------------|------------------|------------------|------------------|
| Bit   | 7                 | 6                 | 5        | 4        | 3                | 2                | 1                | 0                |
| Field | MODE <sub>1</sub> | MODE <sub>0</sub> | Reserved | Reserved | OBS <sub>3</sub> | OBS <sub>2</sub> | OBS <sub>1</sub> | OBS <sub>0</sub> |

Data Type: Bit field

USAGE: Register 0x2e provides bits that are set every frame. It can be used during EFTB testing to check that the chip is running correctly. Writing anything to this register will clear the bits.

| Field Name          | Description   |
|---------------------|---|
| MODE <sub>1-0</sub> | Mode Status: Reports which mode the sensor is in.<br>00 = Run<br>01 = Rest1<br>10 = Rest2<br>11 = Rest3 |
| OBS <sub>3-0</sub>  | Set every frame   |

---

**Reserved** Address: 0x2f-0x39

---

**POWER\_UP\_RESET** Address: 0x3a

Access: Write Reset Value: Undefined

|       |                  |                  |                  |                  |                  |                  |                  |                  |
|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit   | 7                | 6                | 5                | 4                | 3                | 2                | 1                | 0                |
| Field | RST <sub>7</sub> | RST <sub>6</sub> | RST <sub>5</sub> | RST <sub>4</sub> | RST <sub>3</sub> | RST <sub>2</sub> | RST <sub>1</sub> | RST <sub>0</sub> |

Data Type: 8-bit integer

USAGE: Write 0x5A to this register to reset the chip. All settings will revert to default values.



**Inverse\_Revision\_ID** Address: 0x3e

Access: Read Reset Value: 0xFD

|       |                   |                   |                   |                   |                   |                   |                   |                   |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit   | 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| Field | NRID <sub>7</sub> | NRID <sub>6</sub> | NRID <sub>5</sub> | NRID <sub>4</sub> | NRID <sub>3</sub> | NRID <sub>2</sub> | NRID <sub>1</sub> | NRID <sub>0</sub> |

Data Type: Inverse 8-bit unsigned integer

USAGE: This value is the inverse of the Revision\_ID. It can be used to test the SPI port.

---

**Inverse\_Revision\_ID** Address: 0x3f

Access: Read Reset Value: 0xF2

|       |                   |                   |                   |                   |                   |                   |                   |                   |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit   | 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| Field | NPID <sub>7</sub> | NPID <sub>6</sub> | NPID <sub>5</sub> | NPID <sub>4</sub> | NPID <sub>3</sub> | NPID <sub>2</sub> | NPID <sub>1</sub> | NPID <sub>0</sub> |

Data Type: Inverse 8-bit unsigned integer

USAGE: This value is the inverse of the Product\_ID. It can be used to test the SPI port.

---

**Motion\_Burst** Address: 0x42

Access: Read Reset Value: Any

|       |                 |                 |                 |                 |                 |                 |                 |                 |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit   | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
| Field | MB <sub>7</sub> | MB <sub>6</sub> | MB <sub>5</sub> | MB <sub>4</sub> | MB <sub>3</sub> | MB <sub>2</sub> | MB <sub>1</sub> | MB <sub>0</sub> |

Data Type: Various

USAGE: Read from this register to activate burst mode. The sensor will return the data in the Motion register, Delta\_Y, Delta\_X, Squal, Shutter\_Upper, Shutter\_Lower, and Maximum\_Pixel. A minimum of 3 bytes should be read during a burst read. Reading the first 3 bytes clears the motion data.

For product information and a complete list of distributors, please go to our website: [www.avagotech.com](http://www.avagotech.com)

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